

Development of a high-bandwidth waveform processing system using RFSoc

S. Takeshige,^{*1} H. Baba,^{*2} K. Kurita,^{*1} Y. Togano,^{*1} J. Zenihiro,^{*3} and Y. Hijikata^{*3}

We are developing a real-time digital signal processing unit using a GHz-band flash-type analog-to-digital converter (FADC) to establish the next-generation data acquisition system at RIBF. In experiments using radioactive ion (RI) beams, it is necessary to identify each particle. For this purpose, detectors are installed along the beam line, and signals are acquired on an event-by-event basis. However, as the amount of beams increases, conventional CAMAC/VME ADC/TDC modules become a measurement bottleneck owing to its slow processing rate. For germanium detectors, real-time digital signal processing is applied using 100-MHz FADCs instead of conventional ADC/time-to-digital converter (TDC) modules.¹⁾ However, 100 MHz is insufficient for signals with high-frequency components such as those from plastic scintillators used as beam-line detectors.

The Xilinx radio frequency system-on-chip (RFSoc) has been commercially available since 2018. It is a device designed for 5 G communication and integrates an FADC (up to 5 GHz) and field-programmable gate array (FPGA) on one chip. This RFSoc has the potential to perform real-time digital signal processing for high-intensity RI-beam experiments.

In this study, we used the Xilinx ZCU111 evaluation kit²⁾ (Fig. 1). This kit has 8 channels of ADC inputs, 8 channels of DAC outputs, and 20 channels of general-

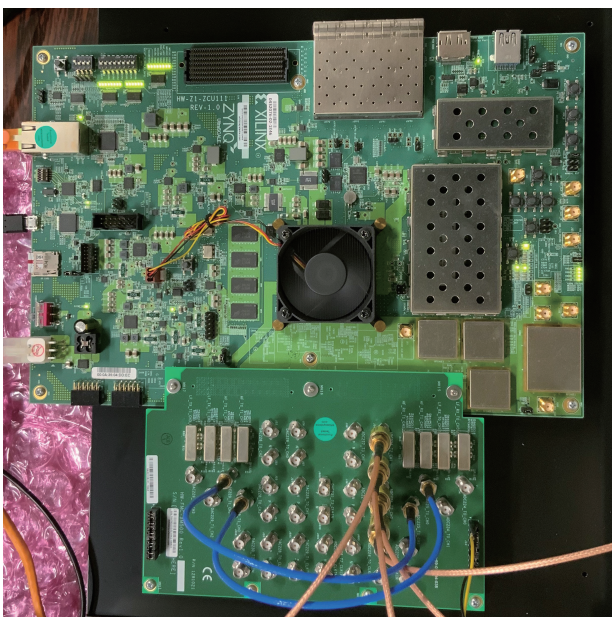


Fig. 1. Xilinx ZCU111 evaluation kit used for development.

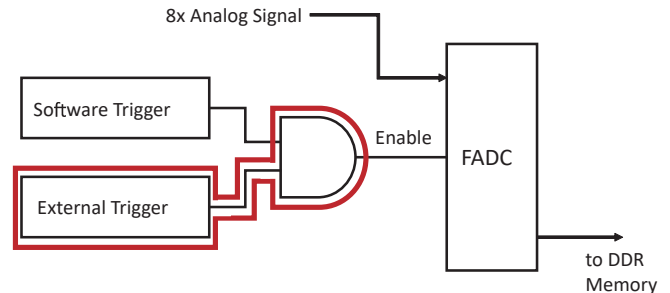


Fig. 2. Block diagram of the implemented external trigger function. The bold line shows the implemented part.

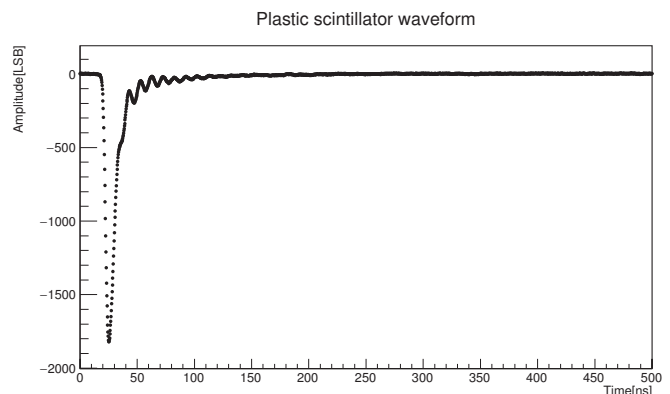


Fig. 3. An example of an acquired plastic scintillator waveform.

purpose I/O ports. The specifications of the ADC input are as follows: 100 Ω differential impedance, AC coupling, and 1 V_{ppd} voltage range. The maximum sampling frequency of the ADC is 4.096 GHz, and the resolution is 12 bits.

As it is not possible to implement external triggers with sample FPGA firmware provided by Xilinx, we added external trigger function. The block diagram is shown in Fig. 2. When data acquisition is started, a software trigger is enabled. At this time, when an external trigger is issued, digitized data are stored in memory. Finally, data are retrieved by a PC via the network. An example of an acquired plastic scintillator waveform is shown in Fig. 3.

We added an external trigger function to the RFSoc device and confirmed that it works successfully. Basic studies such as the measurement of the timing resolution are in progress.

References

- 1) J. -P. Martin *et al.*, IEEE Trans. Nucl. Sci. **55**, 84 (2008).
- 2) Xilinx, Zynq UltraScale+ RFSoc ZCU111 Evaluation Kit, <https://japan.xilinx.com/products/boards-and-kits/zcu111.html>.

^{*1} Department of Physics, Rikkyo University

^{*2} RIKEN Nishina Center

^{*3} Department of Physics, Kyoto University