Fast beam interlock system for BigRIPS separator

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The fast beam interlock system for the BigRIPS separator[1] was designed and constructed in 2014 and has been in operation since then to protect the beam line equipment from hitting the misaligned intensive primary beams due to magnet failure. The interlock system utilizes four compact RIO systems (cRIO) of National Instrument Co. Ltd. as the processing modules and continuously monitors the power supplies of 34 magnets placed at the primary beam line and BigRIPS, where a primary beam is transported. The current monitor signals from the power supplies are digitized by ADCs in cRIO every 2 μs and compared with the pre-defined upper and lower limits. A fault signal is generated if the digitized values are beyond these limits. The fault signals are merged into other fault signals and fed to the beam chopper system to cut off the beam. The total response time, which is defined as the time between an analog signal drift and a beam stopping at the third focus (F3) of BigRIPS, was $\sim$200 μs for a ^{48}Ca 345 MeV/nucleon beam.

During the operation of fast interlock system, the original system was found to be weak for the fluctuation of input noises. The noise of current monitor signals is not always stable. If the noise suddenly increases, the interlock system detects it as the drift of the current output and generates the fault signal. The beam is then stopped by the beam chopper. This happens a few times per day during the beam time.

The inspection of the current monitor signal using a digital storage type oscilloscope revealed the existence of two types of noise: a bi-polar ringing-like noise with high frequency (more than 2 MHz), a short unipolar pulse whose duration is approximately 20 μs. The latter was created with the discharge of electrostatic deflector EDC of the SRC. To prevent the detection of these noises, noise filters are inserted in the analog input lines.

One such noise filter is a passive low-pass filter. EMI filtering capacitor EMIFIL DDS1 0.022 μF of Murata was installed at the current monitor outputs of magnet power supplies. The moving average method was also implemented after the ADC of cRIO system, considering the average of 2 to 16 successive digital values from the ADC. Because ADC provides the converted value every 2 μs, the averaging takes place between 4 and 32 μs. By installing the EMI filter and taking the average of 16 successive AD values, the ringing like noise was completely eliminated from the system. However, the short pulse noise could still be detected because the pulse was slower than the EMI filter and unipolar pulses were not eliminated by averaging.

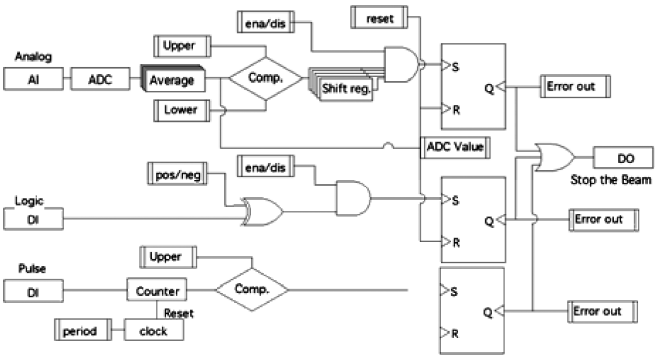

Fig. 1. Logic diagram of upgraded fast interlock system.

To eliminate the short pulse noise, a time-over-limit detection mechanism was further added to the interlock logic. This was accomplished by installing a bit-shift register on the output of the comparator, which compared the digitized signal and pre-defined limits. Each output of the comparator was stored in the first bit of the bit-shift register. The remaining bits of the register were pre-shifted by one bit before storing the first bit. Thus, the 16 bit register stored 16 successive comparison results. A failure signal was generated when all 16 bits were in the "on" state. With this algorithm, the failure signals were only generated for the input signals whose amplitudes exceeded the limit by 32 μs. Therefore, the deviation of input signals shorter than 32 μs was completely ignored.

The interlock logic was modified as shown in Fig. 1 by modifying the FPGA program code in the cRIO system and no hardware modification was required. The actual modification was performed in April 2018 and since then, the fast beam interlock system has been operated with no noise.

Reference

1) K. Yoshida *et al.*, RIKEN Accel. Prog. Rep. **47**, 169 (2014).

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